

# Thin-body FinFET Powers ICs To Beyond 10nm

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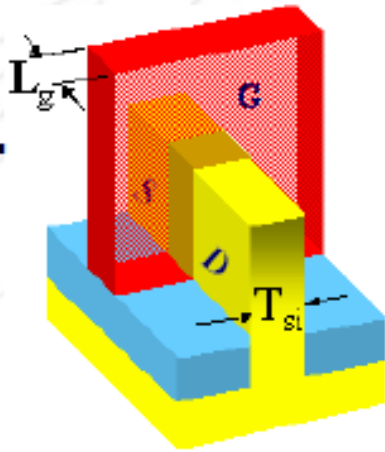
# May 4 2011

## New York Times front page

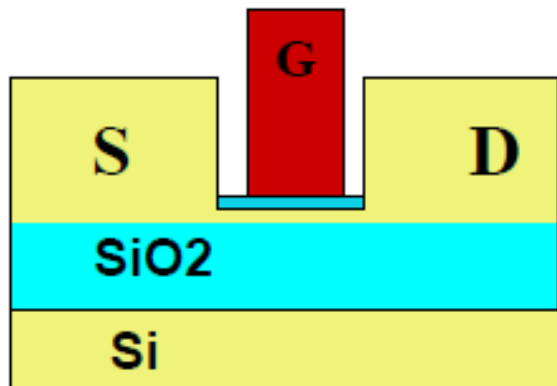
- **Intel will use 3D FinFET at 22nm**
- **Most radical change in decades**
- **There is a competing SOI technology**

# New MOSFET Structures

**FinFET**

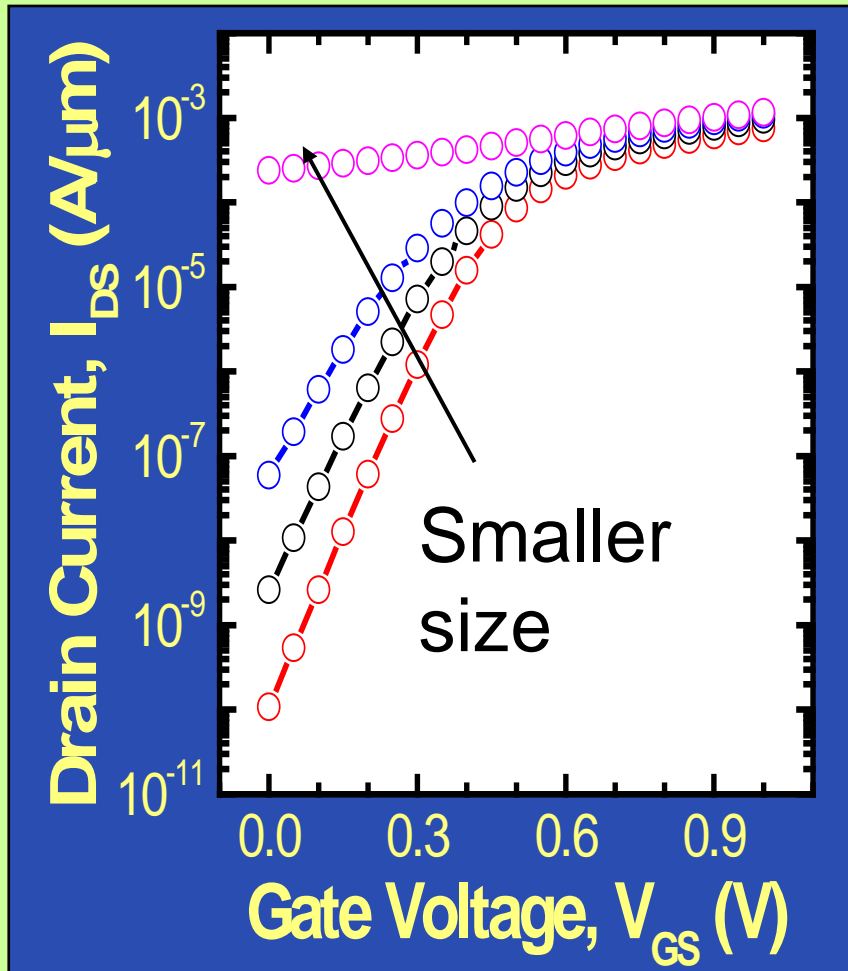


**UTBSOI**



**Ultra Thin Body SOI**

# Good Old MOSFET Nearing Limits



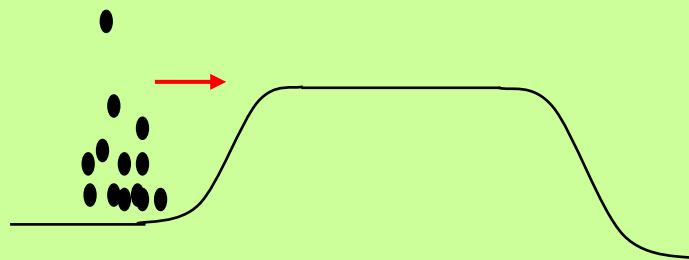
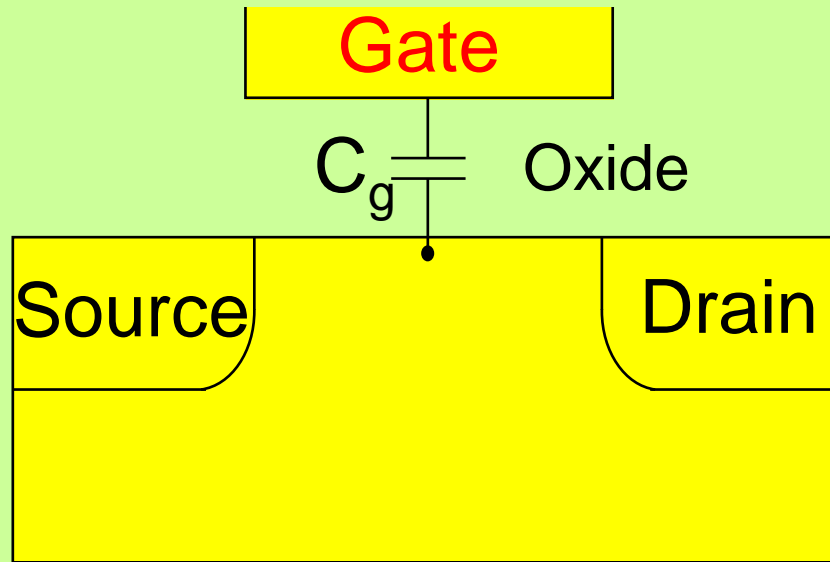
- $I_{off}$  is bad
- Size and dopant variations



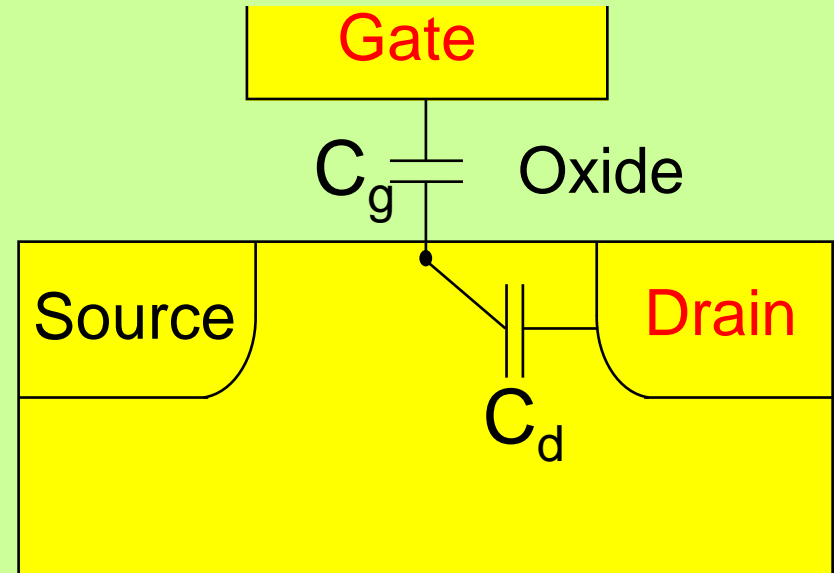
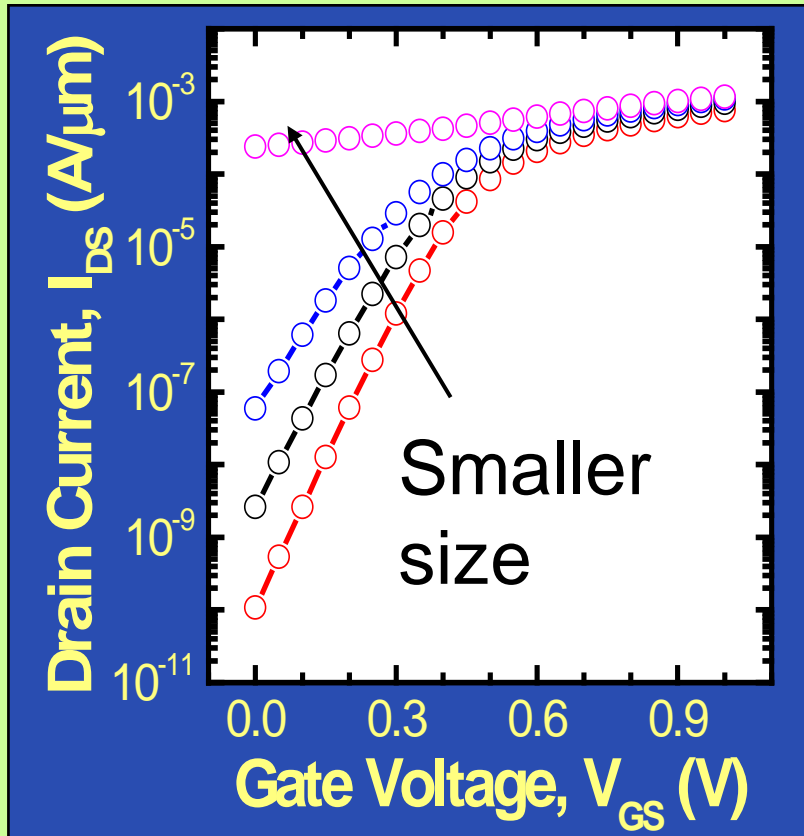
**High  $V_{DD}$ , power, design cost**

**Finally painful enough for change.**

# Long Channel MOSFET

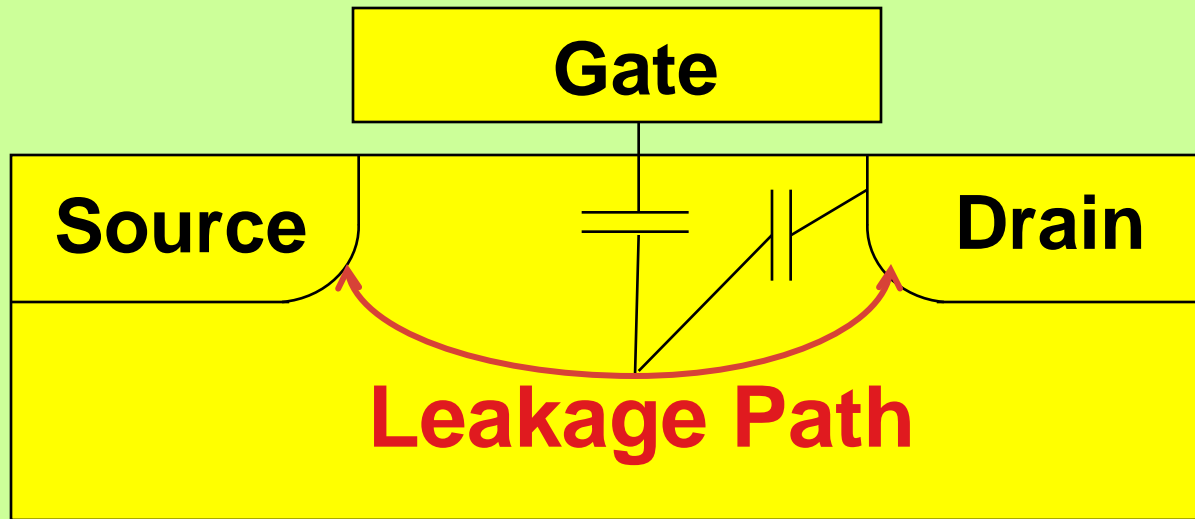


# Why Ioff and Variations Got Worse



**MOSFET becomes “resistor”  
at very small L**

# Making Oxide Thin is Not Enough

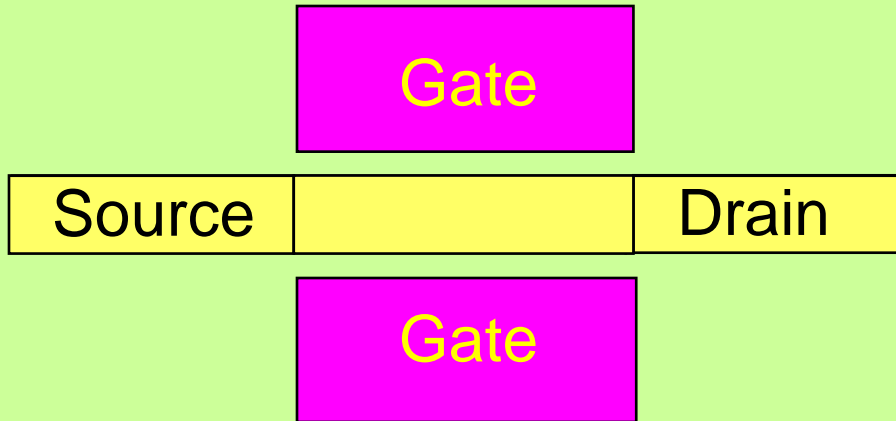


**Gate cannot control the leakage current paths that are far from the gate.**

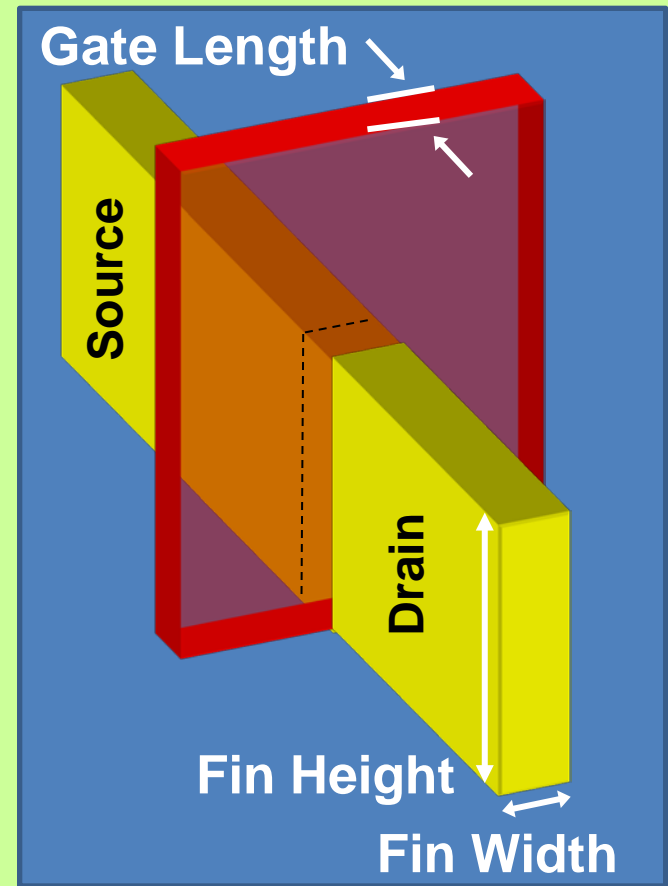
C.Hu, "Modern Semicon. Devices for ICs" 2010, Pearson

# One Way to Eliminate Si far from Gate

A **thin** body controlled by gate from more than one side.



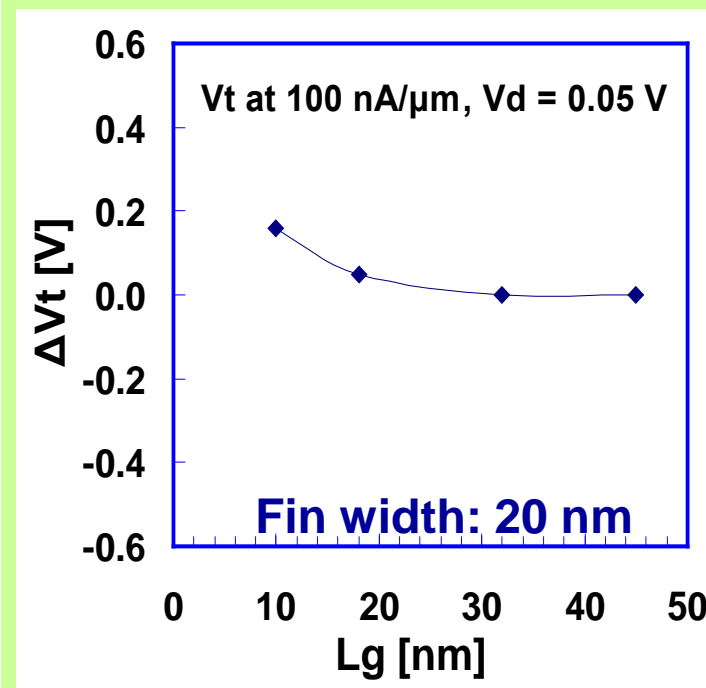
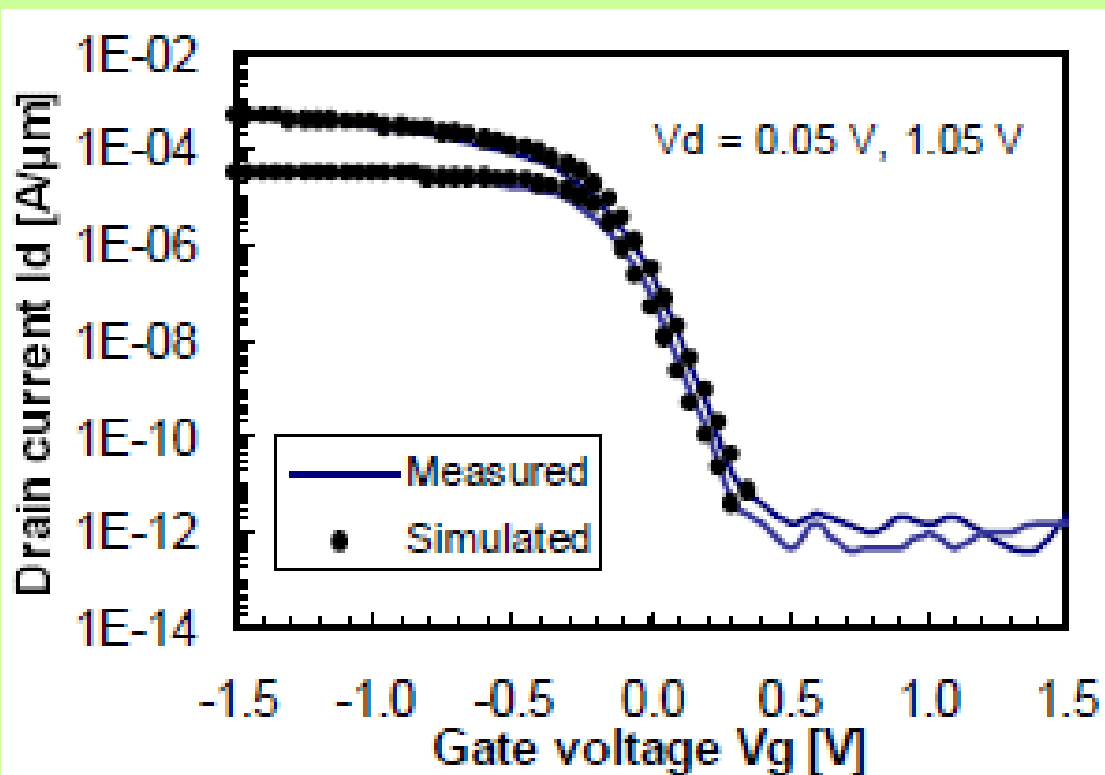
**FinFET body is a thin fin**



N. Lindert et al., DRC paper II.A.6, 2001

# FinFET- 1999

**Undoped Body. 30nm etched thin fin.**  
**Vt set with gate work-function.**



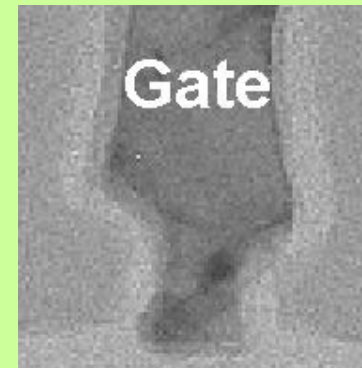
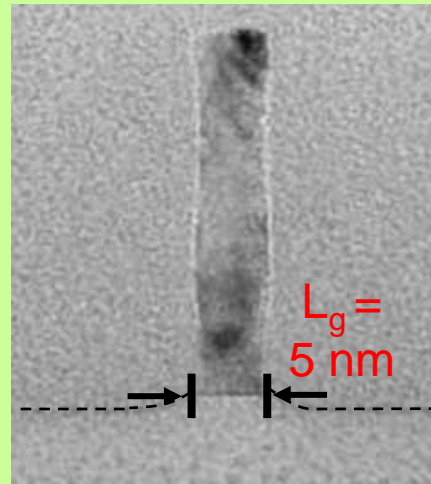
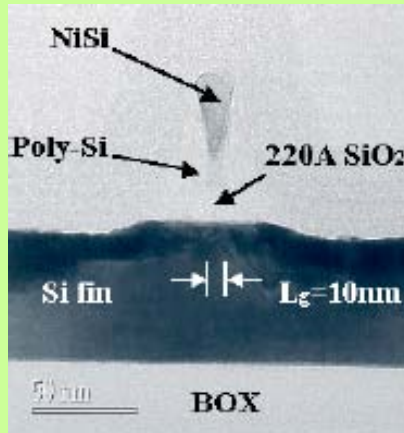
X. Huang et al., IEDM, p. 67, 1999

# FinFET is “Easy” to Scale

10nm Lg AMD  
2002 IEDM

5nm Lg TSMC  
2004 VLSI Symp

3nm Lg KAIST  
2006 VLSI Symp



Leakage is well suppressed if  
**Fin thickness <  $L_g$**

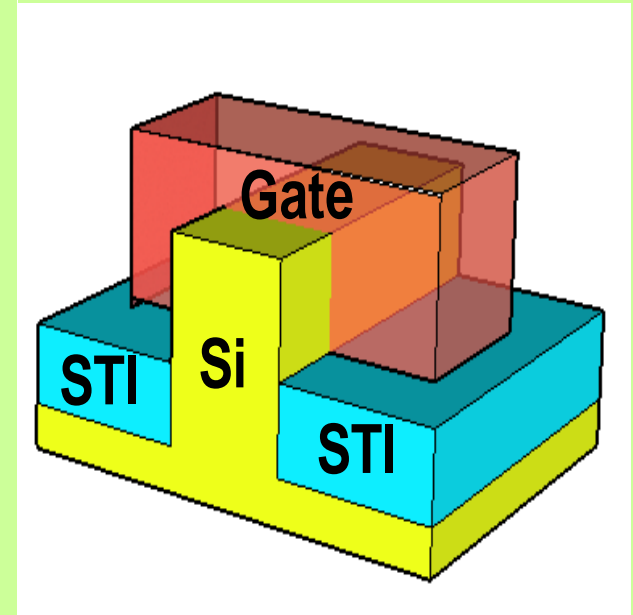
# Two Improvements Since 1999

- **2002** FinFET with thin oxide on fin top.

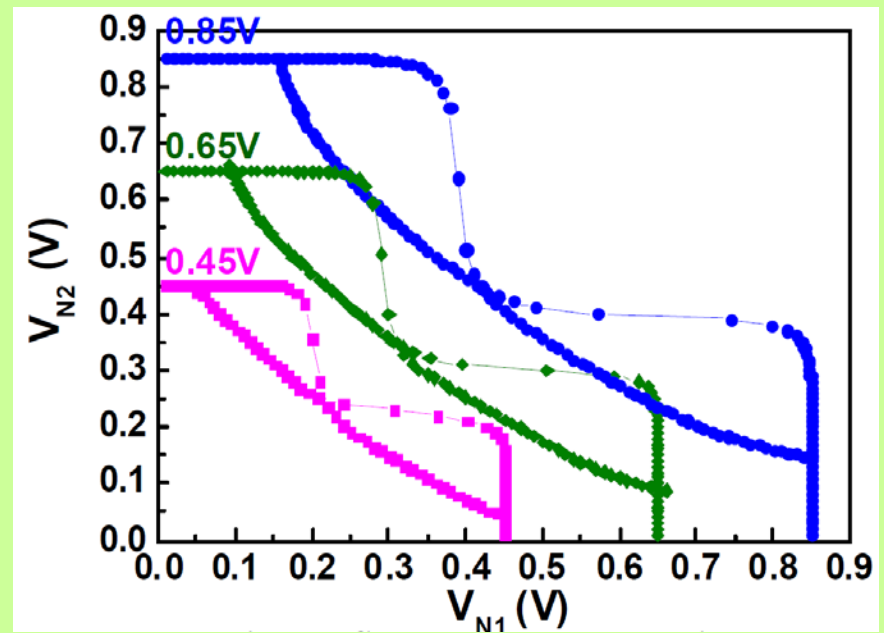
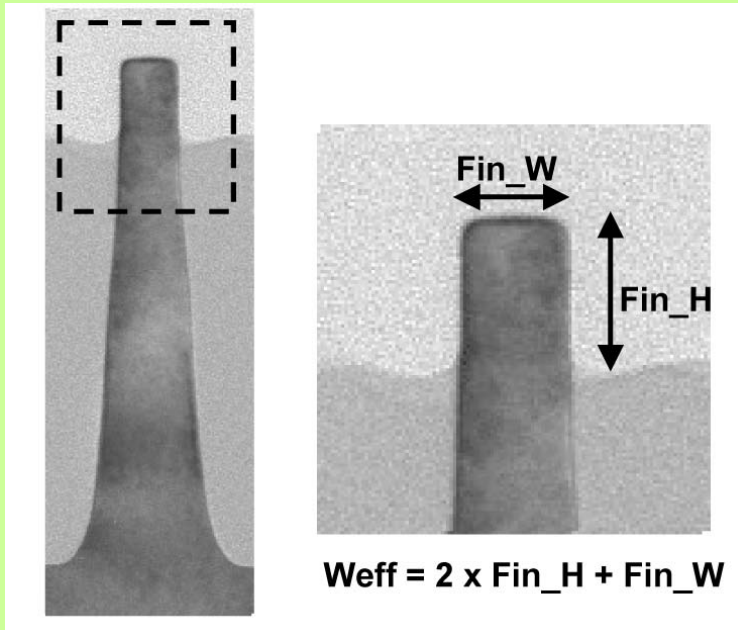
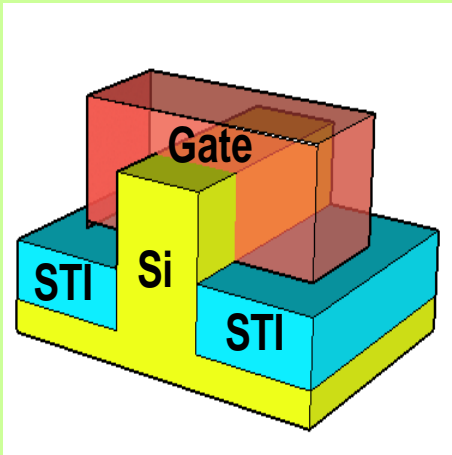
F.L. Yang et al. (TSMC) 2002 IEDM, p. 225.

- **2003** FinFET on bulk substrate.

T. Park et al. (Samsung) 2003 VLSI Symp. p. 135.

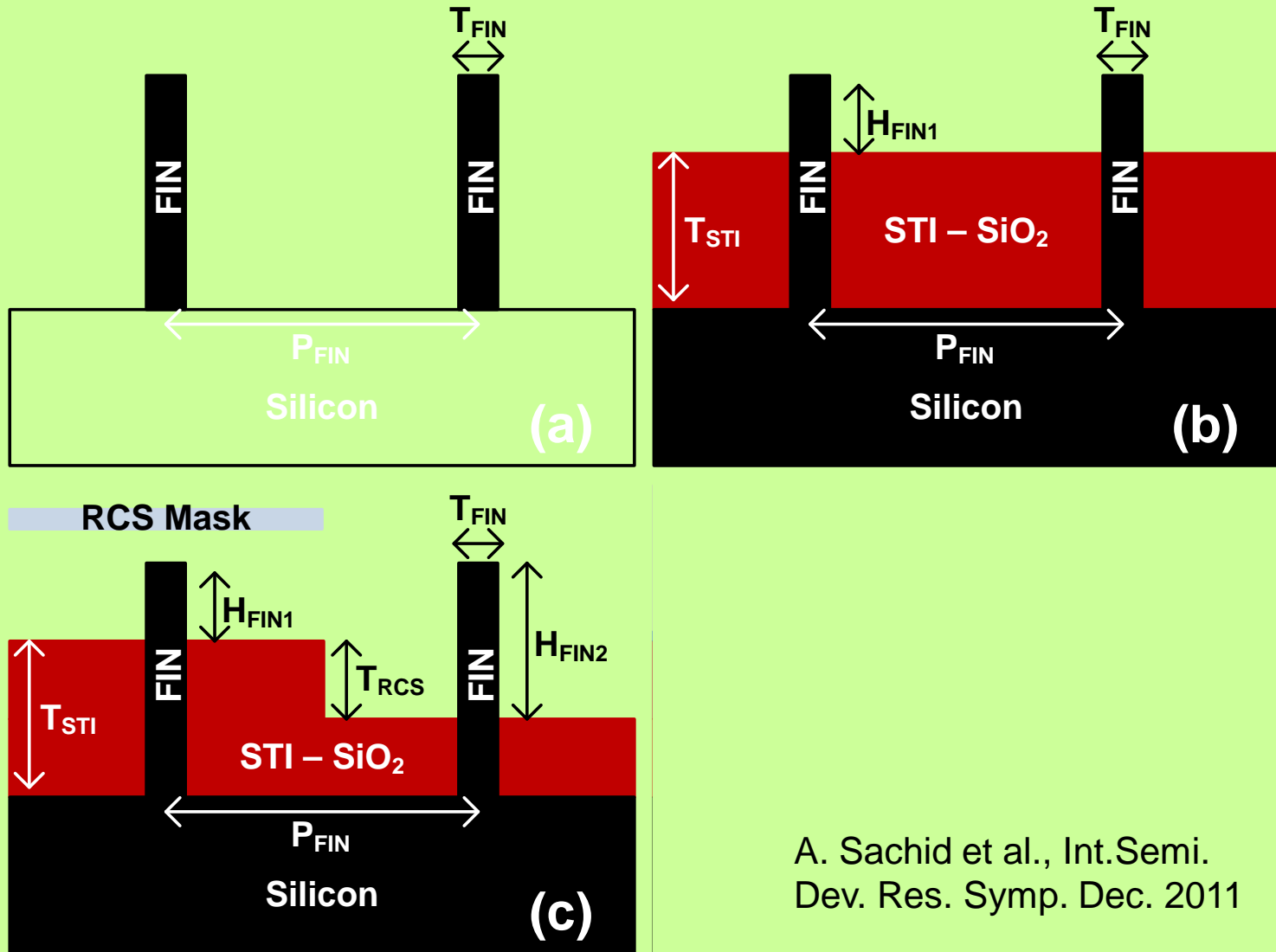


# State-of-the-Art FinFET



20nm Hi Perf  
C.C. Wu et al.,  
2010 IEDM

# Multiple Fin Heights

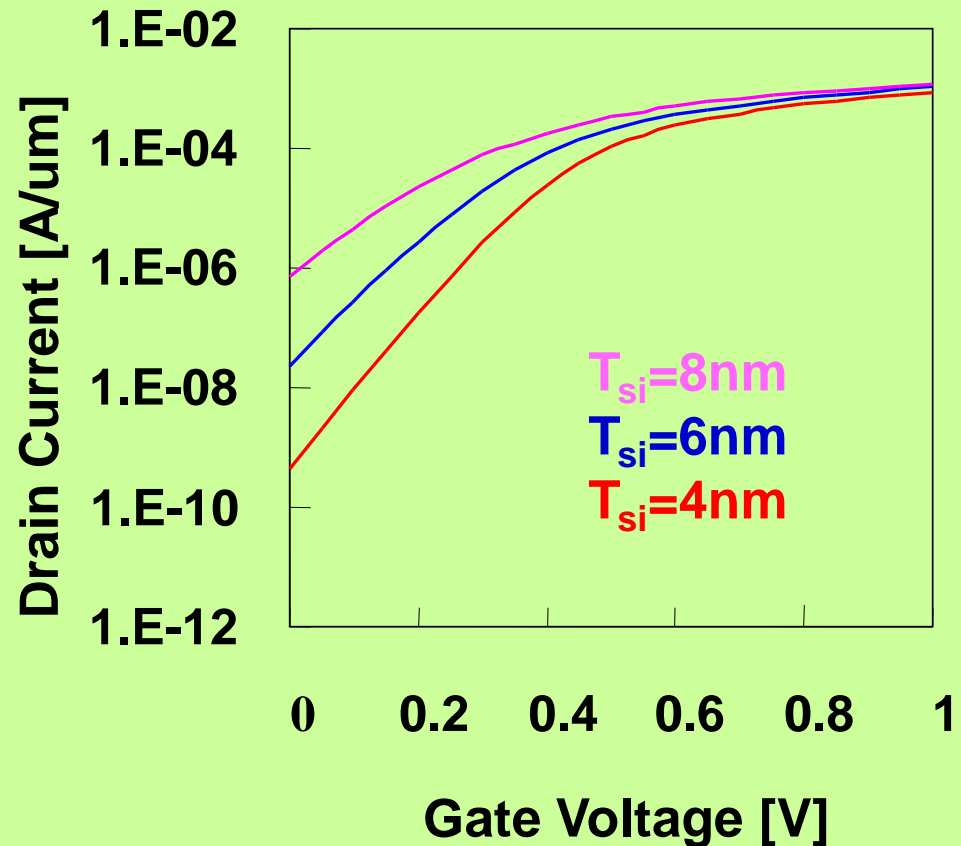
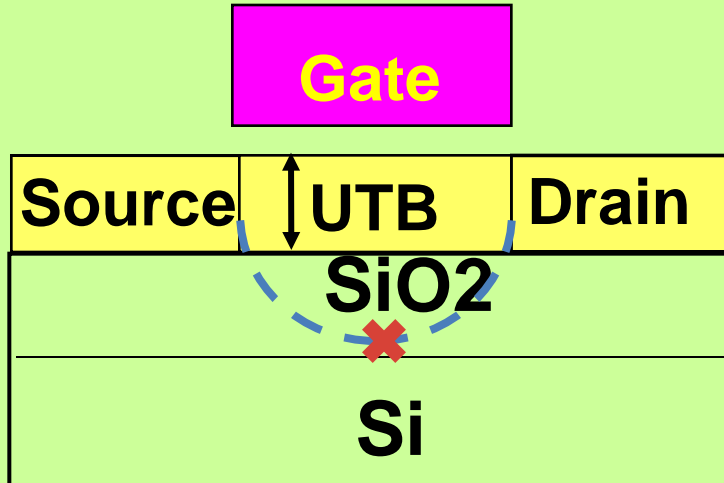


A. Sachid et al., Int.Semi.  
Dev. Res. Symp. Dec. 2011

# 2nd Way to Eliminate Si far from Gate

## Ultra-thin-body SOI (UTB-SOI) →

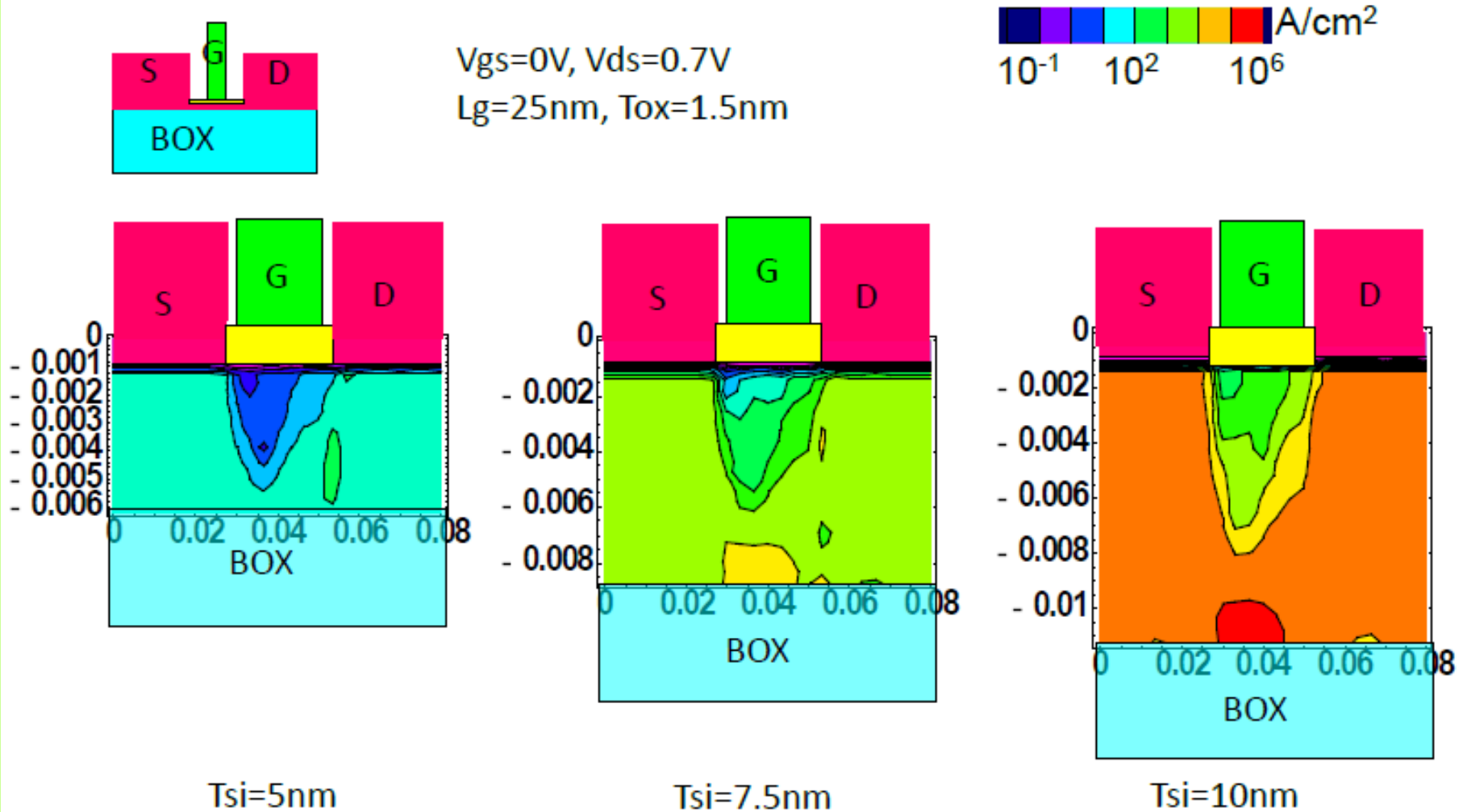
No leakage path far from the gate.



Y-K. Choi, IEEE EDL, p. 254, 2000

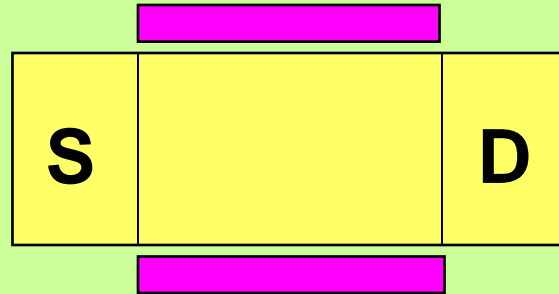
# Most Leakage Flows >5nm Below Surface

## Leakage Current Density



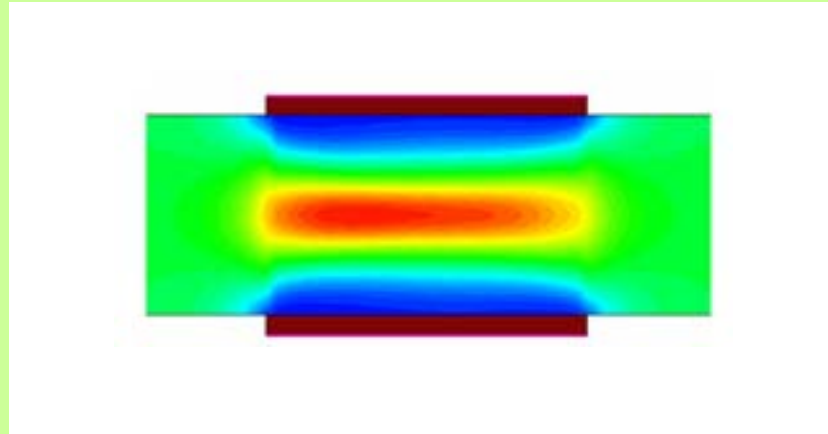
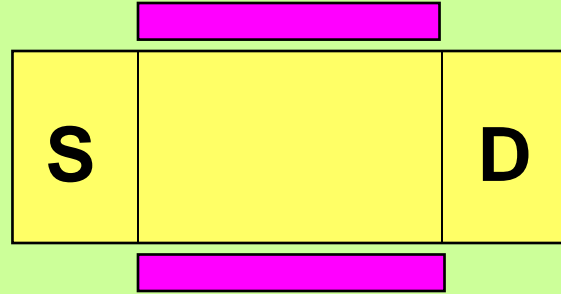
Y-K. Choi et al., IEEE Electron Device Letters, p. 254, 2000

# FinFET's Worst Leakage Path



C.Hu, "Modern Semicon. Devices for ICs" 2010, Pearson

# FinFET's Worst Leakage Path

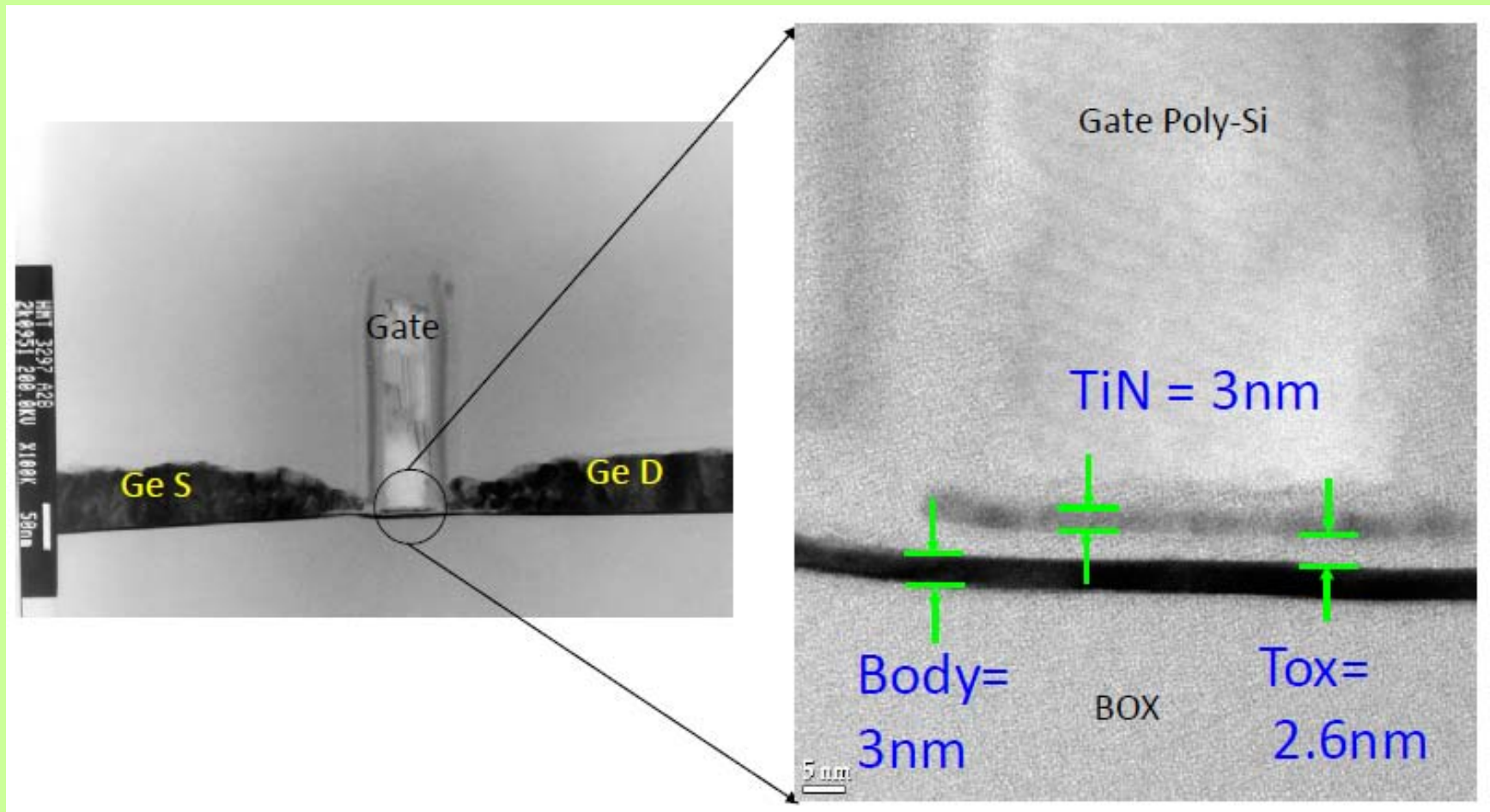


**Body thickness is the new scaling parameter.**

C.Hu, "Modern Semicon. Devices for ICs" 2010, Pearson

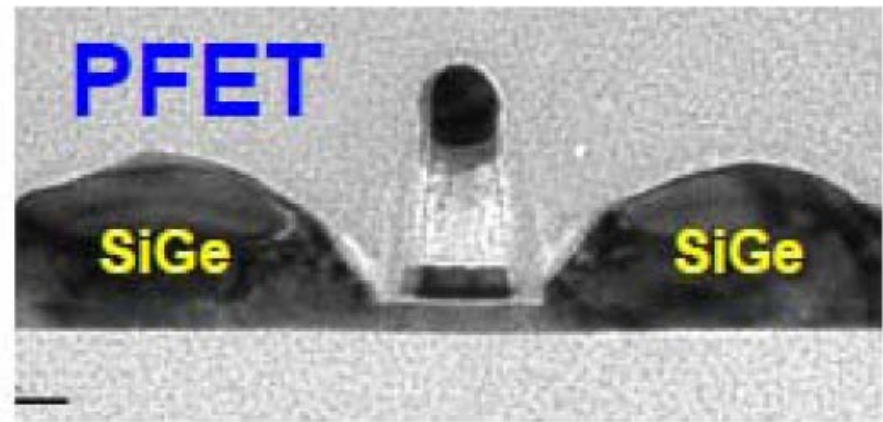
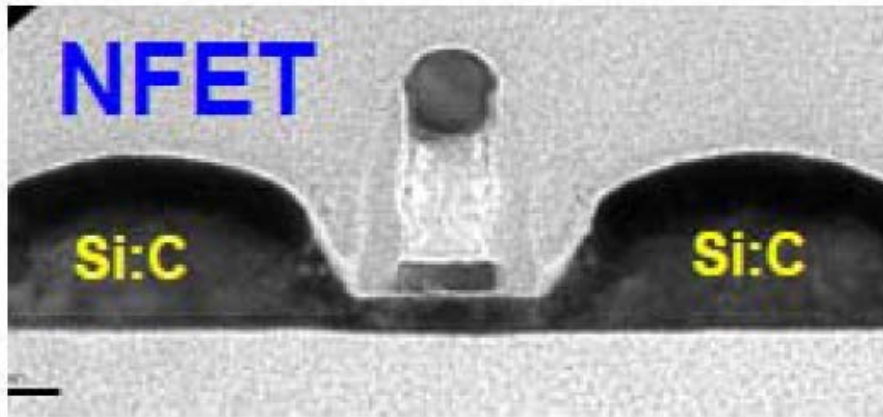
# 2001 UTB-SOI

## 3nm Silicon Body, Raised S/D



Y-K. Choi et al, VLSI Tech. Symposium, p. 19, 2001

# 2009 State-of-the-Art 5nm Body UTB-SOI



ETSOI, IBM

K. Cheng et al, IEDM, 2009

Other Names:

FDSOI

UTBB-SOI

# Both Thin-Body Transistors Provide

- Higher speed and lower leakage
  - Lower  $V_{dd}$  and power
  - Further scaling and lower cost
- 
- Better  $S$  &  $V_t$  and less variations
  - No random dopant fluctuation.
  - Better mobility, especially for future subthreshold design.

# Main Differences

- **FinFET** body thickness  $\sim L_g$ .

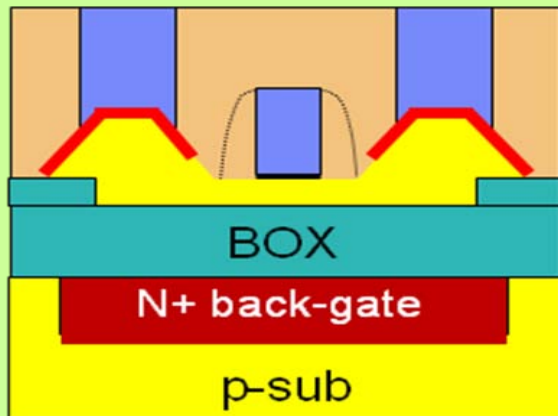
Investment by fab.

**UTBSOI** thickness  $\sim 1/3 L_g$ .

Investment by Soitec.

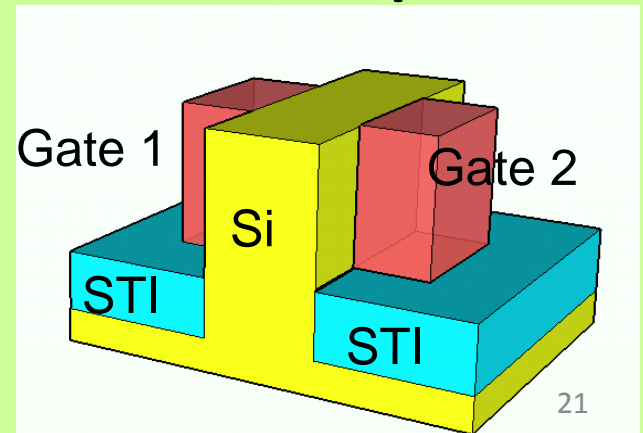
- **FinFET** has larger Ion.

**UTBSOI** has a good back-gate bias option.



**UTBSOI**

**FinFET**



# Outlook

- **FinFET** usage starts at 22nm by Intel and 14nm by foundries--- to beyond 10nm.
- ST will use **UTBSOI** to gain market from regular CMOS at 28nm, 20nm...
- Competition will bring out the best of both.